Development of a Novel Epitaxial-Layer Segmentation Method for Optoelectronic Device Fabrication

Paulo H. O. Rappl and Patrick J. McCann

***Abstract*—This letter describes the development of a new process for segmenting epitaxial-layer material and fabricating cleaved-cavity lasers. The technique, which involves growth substrate removal and use of a novel epitaxial-layer cleaving tool, is applicable to a variety of different materials and devices. In this letter, IV–VI semiconductor epitaxial layers grown by molecular beam epitaxy on silicon (111) substrates with a water-soluble barium fluoride buffer layer were used. The layers were metallurgically bonded to the rectangular tips (500 $\times$ 1040 μm) of copper bars held together by a small vise apparatus, the substrate was removed by dissolving the barium fluoride buffer layer in water, and the copper bars were separated by releasing the vise assembly. Current versus voltage characterization of separated p-n junction IV–VI epilayer structures on the tips of the copper bars showed nonlinear behavior with a forward bias current onset voltage $\sim$250 mV, a value consistent with the room temperature bandgaps of the IV–VI alloys used. These results demonstrate the utility of this technique for obtaining epitaxial-layer structures with typical cleaved-cavity in-plane laser dimensions.**

***Index Terms*—Current versus voltage, epitaxial liftoff, IV–VI semiconductors, laser fabrication, p-n junction.**

I. Introduction

FABRICATION OF in-plane lasers from epitaxially grown materials has traditionally involved a wafer cleaving procedure to obtain Fabry–Pérot resonant cavity structures. This procedure has not been significantly improved upon since it was first developed in the early 1960s. Eliminating this cleaving step has, in fact, been one of the motivations for developing vertical-cavity surface-emitting lasers (VCSELs). Development of a technique that allows for the use of a more manufacturable epitaxial-layer cleaving procedure would help make in-plane laser fabrication more attractive. This is important since such lasers are still preferred over VCSELs for many applications because of the higher emission powers associated with longer cavity lengths. Opportunities exist to develop such a technique with the use of growth-substrate removal procedures, which have been developed for various materials systems. These procedures involve the use of a selectively etchable AlAs release layer for III–V materials [1], a water soluble BaF_2 buffer layer for IV–VI materials [2], [3], and interfacial laser decomposition for gallium-nitride-based materials [4], [5]. Growth substrate removal allows various ways to manipulate epitaxial-layer material, one of which involves a copper plate assembly as an alternative substrate form to obtain slabs of cleaved epitaxial-layer material [6]. In this letter, we describe an advancement of this method in which copper bars are used instead of plates. The technique yields epitaxial-layer material with dimensions typical of in-plane cleaved-cavity lasers. The procedures described are applicable to any materials system for which the growth substrate can be removed. A key advantage of using this new procedure for laser fabrication is the potential for lower production costs since many laser devices can be obtained in a single step. In addition, this laser-fabrication method [7] enables enhanced active-region heat dissipation since the laser structure alone can be sandwiched between two copper heat sinks without an intervening low thermal conductivity growth substrate [8]. The technique, although demonstrated here with IV–VI materials, can be particularly useful for GaN laser fabrication since removal of an insulating sapphire growth substrate allows direct electrical contact to both sides of the device, thus eliminating an etching step and allowing more efficient use of epitaxial-layer material.

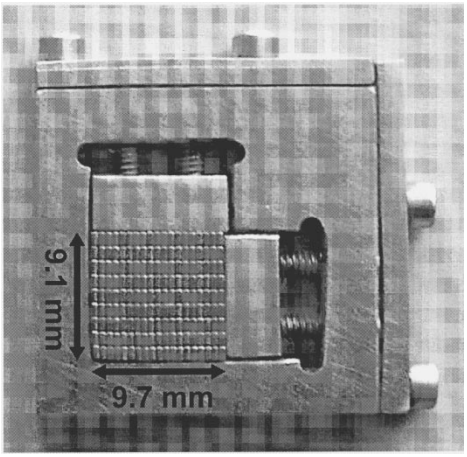

Fig. 1. Photograph of cleaving jig assembly containing 171 copper bars, before nickel and gold metallization, held together in two orthogonal directions with a vise apparatus.

Fig. 1 is a photograph of the cleaving jig assembly [9] used in this work. An array of 171 oxygen-free high-conductivity

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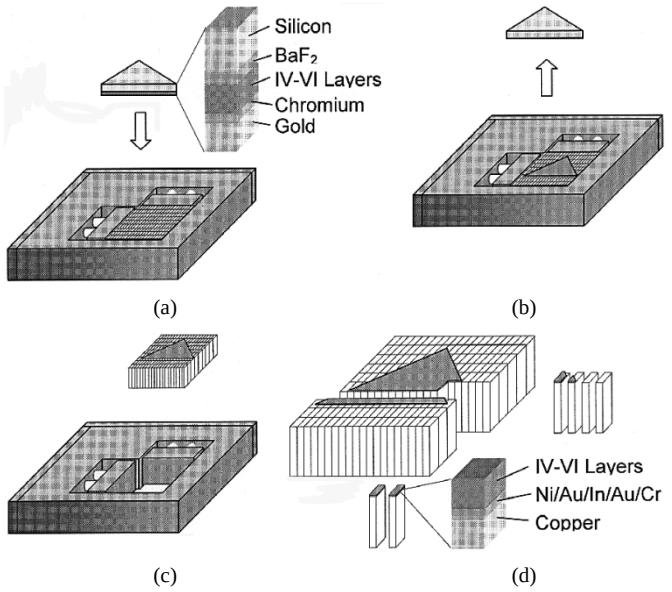

Fig. 2. Procedure for separating epitaxial-layer material. (a) IV–VI semiconductor epitaxial material bonding to tips of copper bars. (b) Growth substrate removal by dissolving MBE-grown BaF_2 buffer layer in water. (c) Copper bar assembly removal from vise apparatus. (d) Copper bar (and epitaxial-layer material) separation.

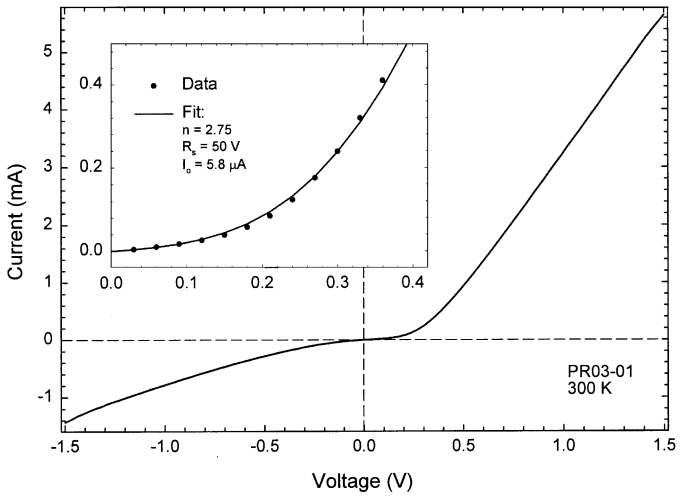

Fig. 3. Current-versus-voltage relationship for MBE-grown IV–VI semiconductor p-n junction structure on the tip of a copper bar. Inset highlights low voltage region and fitting parameters for (1).

copper bars in a 9 × 19 matrix filled an area of about 9.7 × 9.1 mm inside a stainless steel vise assembly. The vise is designed to squeeze the copper bars, each of which is 500 μm × 1040 μm × 4 mm, in two orthogonal directions. After polishing, a thermal evaporation system was used to deposit 500 Å of nickel and 3000 Å of gold onto the surface.

The IV–VI semiconductor epitaxial-layer structure (#W347) was grown by molecular beam epitaxy (MBE) on a (111)-oriented silicon substrate using procedures described in detail elsewhere [10], [11], [13]. The layer structure consisted of a thin (2-nm) CaF_2 layer, a 580-nm-thick BaF_2 layer, a 2.22-μm-thick p-type (Ag doped, p $\sim$ 2.4 × 10^{18} cm^{-3}) $Pb_{0.934}Sr_{0.066}Se$ layer, an undoped (but nominally p-type, p $\sim$ 1 × 10^{17} cm^{-3}, due to selenium overpressure during growth) 525-nm-thick 15-period $Pb_{0.934}Sr_{0.066}Se$–PbSe multiple quantum well (MQW) layer consisting of 10-nm-thick PbSe wells, and a 2.03-μm-thick n-type (Bi doped, n $\sim$ 8 × 10^{18} cm^{-3}) $Pb_{0.934}Sr_{0.066}Se$ layer. The structure was capped with a thin (18-nm) layer of n^+-type (Bi doped, p $\sim$ 1 × 10^{19} cm^{-3}) PbSe. After removal from the MBE system, the 3-in diameter wafers were cleaved along the (111) planes of the silicon substrate to form triangular chips with approximately 1-cm-long edges. The epilayer surfaces of these chips were then metallized with 300 Å of chromium followed by 3000 Å of gold.

The bonding procedure, Fig. 2(a), was performed by setting the chip metallized epilayer side down onto the metallized copper bar portion of the cleaving jig assembly while the assembly was held at 200 °C in laboratory atmosphere on a hot plate. Immediately before contact, a small amount of indium, enough to form an approximately 10-μm-thick layer over a 1-cm^2 area, was placed on the gold-coated copper bar portion. With a melting point of 157 °C, the indium forms a liquid wetting layer and promotes adhesion between the epilayer and copper through formation of intermetallic compounds that include In_2Au [6]. The amount of indium used is critical since too little will lead to rapid intermetallic alloy formation before the entire bonding interface is wetted, while too much will cause indium extrusion which can coat the sides of the exposed epitaxial-layer structure and limit the ability to dissolve the BaF_2 release layer. Bonding was completed by applying a small amount of uniform pressure to the back side of the chip while the hot plate was allowed to cool to room temperature.

Growth substrate removal, Fig. 2(b), involved simple immersion of the bonded assembly in magnetically stirred deionized water held at room temperature. This procedure selectively dissolves the BaF_2 buffer layer incorporated into the MBE-grown structure without significantly affecting any of the other materials. The bonded assembly was suspended, MBE sample-side down, with no force applied to the substrate other than gravity. Release time depends on the BaF_2 buffer-layer thickness, which was about 24 h for the 0.58 μm thickness used in this work. After growth substrate removal, the screws holding the copper bars together were loosened allowing the copper bar assembly to be removed as a complete block, Fig. 2(c). The bars were then separated, first row-by-row and then individually, using a razor blade. This separation step is depicted in Fig. 2(d).

Selected copper bars with pieces of epilayer material covering the entire tip were electronically characterized using a dc voltage source/current meter instrument (Hewlett-Packard 4140-B). Electrical contact to the exposed p-type $Pb_{0.934}Sr_{0.066}Se$ layer (originally adjacent to the BaF_2 buffer) was made by cold pressing and indium-coated wire to the surface. Contact to the n-type $Pb_{0.934}Sr_{0.066}Se$ layer was made through the copper bar, which was attached to the epilayer structure through the Ni–Au–In–Au–Cr bonding medium.

Fig. 3 shows a typical current-versus-voltage relationship obtained at room temperature for a IV–VI semiconductor p-n junction structure prepared using the procedure described above. A clear nonlinear I–V characteristic with a forward bias current onset voltage $\sim$250 mV, a value consistent with the room temperature bandgaps of the IV–VI alloys used, is observed.

A strong series resistance component to current flow, however, is indicated by the nearly linear I–V relationship at potentials greater than 0.5 V. Equation (1) is a modification of the p-n junction diode I–V relationship for when the potential drop across the p-n junction V_j is affected by a series resistance R_s. A good fit to the measured data in the 0 to ∼400 mV

$$I = I_\circ \left[\exp \frac{q\,(V_j - IR_s)}{nkT} - 1 \right] \tag{1}$$

forward bias range (see inset in Fig. 3) was obtained for a series resistance (R_s) of 50 Ω, a reverse bias saturation current (I_o) of 5.8×10^{-6} A ($J_o = 1.12$ mA/cm^2), and a p-n junction ideality factor (n) of 2.75. Note that the measured reverse bias saturation current is much larger than the fitted value of 5.8 μA. The additional measured current is likely due to conduction of thermally and optically generated charge carriers since the measurements were performed at room temperature under ambient lighting conditions. The ideality factor of $n = 2.75$ is only slightly larger than the $n = 2.0$ value normally expected for the low voltage regime of a p-n junction [14], where current due to carrier generation and recombination in the depletion region is dominant [15]. Further experiments are needed to help identify the cause of this higher than expected ideality factor. A good fit to the higher current regime was obtained with a reverse bias saturation current of 1.1×10^{-8} A, a series resistance of 184 Ω and a p-n junction ideality factor of 1.08. A higher series resistance is usually expected at higher voltages due to conduction being limited more by transport through the bulk n-type, p-type, and metallic contact regions, while an ideality factor approaching $n = 1.0$ is also normally expected for the higher voltage regime [14] where current due to diffusion is dominant. The R_oA value for this p-n junction was 24.5 Ω · cm^2. Another sample from the same epitaxial-layer structure had the following low voltage parameters: $R_s = 51\ \Omega$, $I_o = 2.9\ \mu$A, $n = 2.50$, and $R_oA = 23.8\ \Omega \cdot$ cm^2. These I–V data clearly show that functional p-n junctions can be obtained using this new method. This method, in fact, provides a simpler way to characterize IV–VI p-n junctions since it does not require the patterning and etching techniques that have been used in prior studies of similar IV–VI device structures [16].

The large series resistances for the structures obtained in this work make them unsuitable for reliable laser operation because excessive Joule heating at high injection currents will lead to rapid device failure. The series resistances associated with the approximately 2-μm-thick n-type and p-type regions are estimated to be much less than 1 Ω each, so it is believed that metallurgical contact resistance is the primary cause of the large series resistances. Solutions to reducing R_s include incorporation of O_2 plasma cleaning steps prior to metallization, use of deposited indium bonding layers passivated with noble metal oxidation barriers, and metallization of the exposed p-type layer before copper bar separation. Use of a large work function metal such as nickel ($q\Phi_m = 4.9$ eV) for the p-type contact should make a good ohmic contact. Indium ($q\Phi_m = 4.12$ eV) likely formed a Schottky barrier with the p-type side of the device, and this could have contributed significantly to the observed large R_s values.

In summary, a new technique suitable for in-plane laser fabrication has been demonstrated. Involving epitaxial-layer structure bonding to a copper block assembly, growth substrate removal, and segmentation by separating the copper blocks, it was successfully used to obtain 500 × 1040 × 4.77-μm-thick MBE-grown IV–VI semiconductor p-n junction structures on the tips of the copper bars. Theoretical fits to measured I–V data allowed extraction of p-n junction device parameters. Further development of this new laser-fabrication method promises to enable a more manufacturable procedure for obtaining in-plane diode lasers with the added benefit of improved active-region heat dissipation. Future work includes improvement of the metallurgical bonding procedure to increase yield and decrease contact resistance, electron microscope evaluation of cleaved facets, measurement of mid-infrared electroluminescence from MBE-grown IV–VI MQW structures, and extension of the technique to other materials such as GaN-based semiconductors for fabrications of blue and ultraviolet light emitting devices.

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